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ACCELERATED TESTING ON THE RELIABILITY OF SEMI-CONDUCTOR ELEMEN--ETC(U)
MAY 78 H GLADYSZ, J KOLODZIEJSKI

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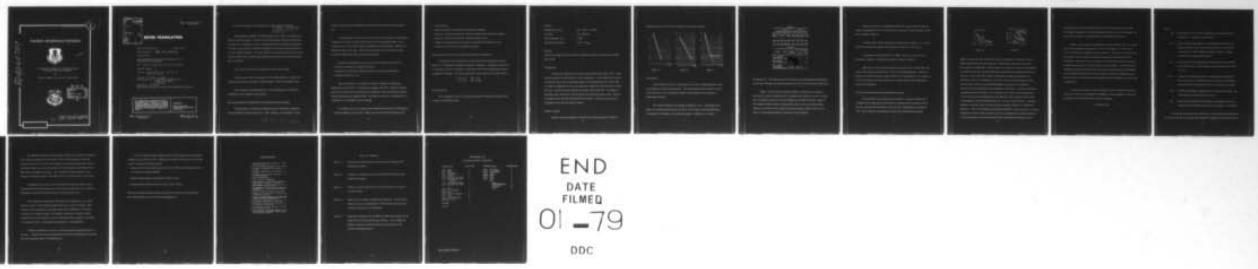

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# FOREIGN TECHNOLOGY DIVISION


## ACCELERATED TESTING ON THE RELIABILITY OF SEMI-CONDUCTOR ELEMENTS

by

Henryk Gladysz and Jerzy Kolodziejski



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By: Henryk Gladysz and Jerzy Kolodziejski

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# Accelerated Testing on the Reliability of Semi-conductor Elements

H. Gladysz, J. Kolodziejski
Industrial Institute of Electronics

Evaluating the reliability of contemporary semi-conductor elements is a serious technical problem. Because of the large sample sizes and long testing periods it is not possible to use the traditional methods of evaluating reliability for failure rates observed actually for transistors and diodes, and particularly for self-contained systems. For this reason for many years now tests have been conducted which aim at elaborating methods which permit an accelerated evaluation of reliability.

One of the most widely used methods is step-stress testing.

The first part of this work shows the use of this method to compare the reliability of a batch of transistors which undergo specific technological tests.

The second part describes the use of accelerated tests to evaluate the reliability of self-contained microsystems.

## Use and Limitations of Reliability Tests Using Step-Stress Testing

The principles of conducting reliability tests by step-stress testing are precisely defined in many works (1-5). Here, however, we would like to draw

attention to the practical possibilities of this method and the factors limiting its use.

The fundamental condition for the correct use of each method of conducting reliability tests with excessive loads predicted as being standard under service conditions is the conformity of failure mechanisms occurring under standard conditions and with an overload. This fact limits the top levels of loads used and decides the sample sizes and necessary testing time.

Generally speaking the results of step-stress testing can be used for:

-- numerical evaluation of reliability indicators,

-- comparison of reliability of different batches, in which technological or structural differences occur.

This second task is, according to a number of writers, the principal application of this method. Young (4) even suggests that tests conducted using the step-stress method can and should be the preliminary stage of reliability testing, and the data which they supply should be the basis for the correct establishment of conditions for conducting long-term testing.

According to this writer step-stress testing should supply the following data:

-- define the highest stress levels--which can be used without developing mech-

anical failures,

-- define the parameters which show the greatest changes,

-- define the connection between the failure mechanism and parameter changes,

-- define the direction of parameter changes during testing,

-- evaluate the sample sizes necessary for long-lasting reliability testing,

-- estimate the real limits for parametric failures.

## Discussion of the Results of Accelerated Testing of Transistors

The purpose of the testing was to verify the manner in which the specific batches of screening tests influence transistor reliability. Testing was conducted on low power siliceous transistors, most often the BF 214-215 (npn) type produced by epiplanar technique. The basic parameters of the transistors are given below

$U_{CBmax} = 30$ V $\quad T'_{jmax} = 175$ °C

$U_{CEmax} = 30$ V $\quad P_{max} = 105$ mW

## Screening Tests

The components chosen were preselected before testing on the basis of the results of the following tests:

Group A

| | |
|---|---|
| temperature cycles | 5X, $-55^{\circ}C \div +125^{\circ}C$ |
| free falls | 3X, 1000 mm |
| moist constantly hot | 4 days |
| preliminary operation | 150 h -- $P_{max}$ |

Group B

optical screening of structures before closing the testing according to the method given in (6).

Testing Plan

Testing was conducted by the step-stress method with a power load. Transistors operated in a WB system at room temperature. Two methods were used to increase the power load in sequential steps--by increasing the current (by 2 mA) at constant voltage (20 V) and by increasing the voltage (by 2 V) with direct current (20 mA). The first step was effected by a power load of 200 mW. The length of individual steps amounted to 16 h in the first test and 40 h in the second. Sizes of all samples were identical and amounted to 50 items. Division into groups and a diagram of the tests are given in Table 1.

Failure Criteria

Failure criteria as applied to evaluate test results are given in Table 2.

Breaks and short-circuits were counted as catastrophic failures.

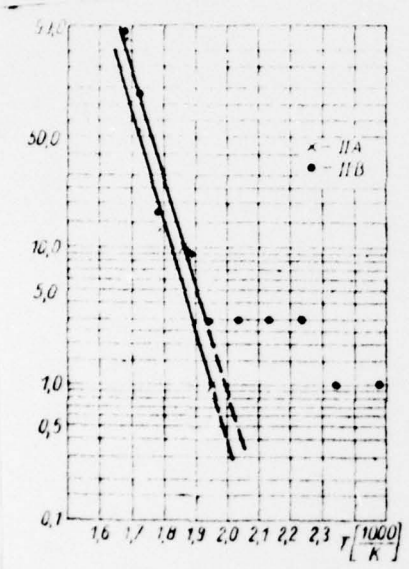


Figure 1.

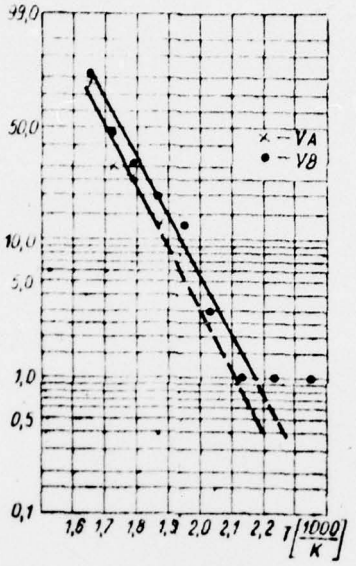


Figure 2.

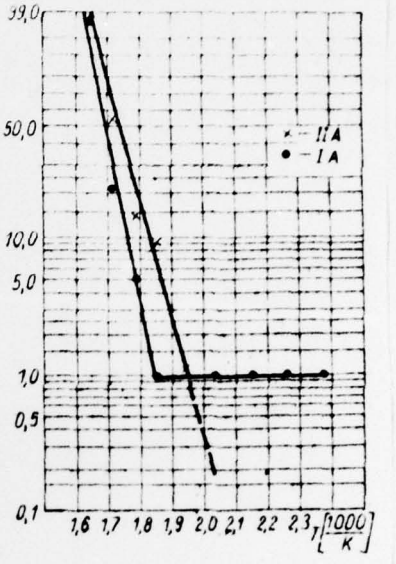


Figure 3.

Test Results

A full analysis of the test results has not yet been completed because of the very expansive experimental material. The results given below should be treated as the first part of the elaboration relative to the principle of the analysis of catastrophic failures.

The results obtained are presented in Figures 1, 2, 3. The graphs were made on a statistical grid selected so that if, on the basis of determining points, the empirical distributant can be plotted straight, it indicates one failure

Table 1

| | Group A | | | | Group B | | | |
|---|---|---|---|---|---|---|---|---|
| | 20 V, 10 mA ... | | 20 mA, 10 V... | | 20 V, 10 mA... | | 20 mA, 10 V... | |
| Test TIME | tested | NOT tested | tested | NOT tested | optic. screen | w/o screen | optic. screen | w/o screen |
| 16h | IA | IB | IIA | IIB | VA | VA | VIA | VIB |
| 40h | IIIA | IIIB | IVB | IVA | VIIA | VIIB | VIIIA | VIIIB |

Table 2

| Parameter | Symbol | Meas. Conditions | Failure Criteria | |
|---|---|---|---|---|
| | | | parameter | Catastroph. |
| Zero current collector-base | $I_{CBO}$ | | 20 µA | 8 µA |
| Zero current emitter-base | $I_{EBO}$ | 4 V | µA | 10 µA |
| Static factor of current multiplication | $h_{21E}$ | $I_C$ = 1 mA<br>$U_{CE}$ = 10 V | $\frac{h_{21E}}{h_{21E}}$ 50% | 10 |

mechanism (7). The temperature of the junctions was determined assuming that the thermal resistance is fixed and identical for the current load and voltage load.

Figure 1 presents the cumulative numbers of failures in a reciprocal function of a junction temperature for a sample which underwent a set of A tests and a comparative sample not tested (sample IIA and IIB according to Table 1). The range of smaller loads is characteristic where, for the untested sample, failures occur much earlier and the practically identical slope of both curves attests to the analogical failure mechanism in both samples.

Figure 2 presents in an analogical manner the results obtained from the sample undergoing the set of B tests and the comparative sample (sample VA and VA according to Table 1).

A similar effect can be observed as in the previous testing, i.e., earlier failures in the untested sample and closeness of slopes of both curves.

A comparison of the results for "voltage" load and "current" load is presented in Figure 3. (samples IA and IIA according to Table 1).

With direct current the first failures were observed at a load of 400 mW, while with constant voltage failures occurred considerably earlier. With loads greater than 400 mW (identical load conditions for both samples) it can clearly be seen that voltage is the factor which more strongly influences the degradation process of transistors.

Accelerated Testing of Self-contained Microsystems

Self-contained semi-conductor microsystems represent a high level of reliability both comparatively with systems realizing similar functions built of discrete elements and absolutely--if you take into consideration the values of "life" time or failure rate attained by these self-contained microsystems.

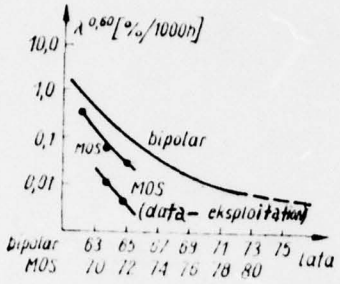


Figure 4.

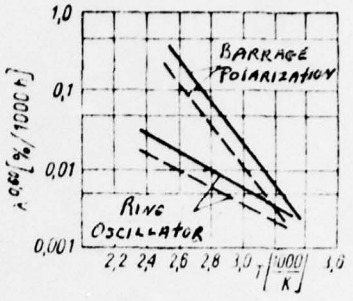


Figure 5.

Figure 4 illustrates this, wherein the values are presented of the failure rate of bipolar and MOS microsystems which are obtained from laboratory tests, and partly from exploitation (8). Failures which are observed in bipolar microsystems are connected chiefly with superficial effects and defects in metallization and connections. On the other hand, failure mechanisms in MOS microsystems are mostly the result of ion migration in an oxide, short-circuits through thin oxide under the gate, defects in the photolithographic processes, slow trapping of carriers in the $Si-SiO_2$ boundary and leakage of connections. In LSI microsystems an additional source of failures can take place in the multi-layered metallization or also in the local overheating of the microsystem, which results from the great close packing of self-contained elements (9). In recent years however, it has been possible to surmount many of these potential reasons for failure or to limit their influence. This occurred thanks to the deeper and fuller understanding of physical phenomena in semi-conductor elements and the acceptance into productive practice of strict demands on the materials used in the technological operations for per-

fection and tolerances in production processes, the cleanliness of rooms and technological equipment, the amount and type of measure-control operations, and also on the introduction of automatization of technological processes.

Thanks to these and other operations the value attained for the $\lambda$ failure rate of self-contained microsystems is--as seen in Figure 4--to the order of $10^{-7} \div 10^{-8}$ 1/h under standard service conditions. At this level of failure rate, with respect to the certainty of reasonable sample sizes and time period of evaluation or control tests, it is necessary to conduct these tests under stricter conditions than foreseen in normal service of microsystems. Such accelerated reliability testing is performed most often with fixed load levels and changeable (or also fixed) testing time (over-stress method). Increased temperature and electrical load are used as loads releasing the failure mechanism, as in the case of transistors.

In many American firms which manufacture semi-conductor elements as well as for reasons of calculating the reliability of army equipment, it has been accepted to use the following semi-empirical equation

$$\lambda_p = \pi_L \pi_Q (C_1 \pi_T + C_2 \pi_E) \qquad (1)$$

where:

$\lambda_p$ -- is the failure rate of a self-contained microsystem expressed in numbers of failures coming in $10^6$ h,

$\pi_L$ -- is the coefficient depending on the experiment held during production of a given type of microsystem (equal to 10 at the start of production or after substantial changes, equal to 1 during controlled and stabilized production),

$\pi_Q$ -- is the figure of merit depending on the kind and scope of testing and screening tests, which the given microsystems passed (from 1 to 150),

$C_1$, $C_2$ -- coefficients defining the degree of complication (complexity) of the micrysystems, depending also on the production technology and function of the microsystem (from several mils to several),

$\pi_E$ -- coefficient (multiplier) regarding the use of the microsystem and environmental conditions (from 0.2 to 10),

$\pi_T$ -- temperature coefficient of acceleration, depending on the technology of the microsystem (from several decimals to a thousand).

If we accept that an electrical load leads to only an additional temperature increase inside the microsystem and establish an exponential distribution for the

"life" time (endurance) of these microsystems, then we get (10)

$$\lambda(T) = \lambda(T_0) \exp\left[-\frac{E_a}{k}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \qquad (2)$$

where:

$\lambda T_0$ -- failure rate at $T_0$ temperature,

$E_a$ -- activation energy of the failure process,

k -- Boltzmann constant

T, $T_0$ -- temperature in K.

For the Weibull distribution with the assumption that the parameter of the shape of the m distribution does not depend on temperature, the equation will have the same pattern but the energy activation must be multiplied by m.

Worked out on the basis of the equation (2) the following are the empirical equations for the temperature coefficient for acceleration (11):

-- for bipolar digital TTL and DTL microsystems

$$\pi_{T1} = 0{,}1 \exp\left[-4794\left(\frac{1}{T} - \frac{1}{298}\right)\right]$$

-- for bipolar and linear MOS microsystems, bipolar digital ECL and digital MOS

$$\pi_{T1} = 0{,}1 \exp\left[-8121\left(\frac{1}{T} - \frac{1}{298}\right)\right]$$

In the ibibliography (12) it is suggested that in the case of TTL microsystems the following multipliers are accepted to calculate the equivalent number of work hours at 55°C as compared with other temperatures. From the series of testing of bipolar ECL digital systems (13) they gave results, as presented in Figure 5.

| Temperature [°C] | 200 | 150 | 125 | 85 | 55 | 25 |
|---|---|---|---|---|---|---|
| Multiplier | 18.7 | 8.0 | 6.8 | 2.5 | 1.0 | 0.37 |

It is evident that operating conditions in a self-contained microsystem in the system of a ring oscillator (or meter) are smoother than in the case of testing at the same temperature, but with a barrage polarization of connections. Similar conclusions are advanced in the work (14) for MOS microsystems. The proper tally for comparative failure rates under various testing conditions are given below

| Testing conditions | Comparative Failure Rate |
|---|---|
| Ring meter 125°C | 100 |
| Ring meter 150°C | 150 |
| Ring meter 75°C | 50 |
| Ring meter 125°C and temp. cycles to -55°C | 230 |
| Storage 125°C with barrage polarization | 190 |
| Storage 150°C | 15 |
| Storage 75°C | 10 |

The influence of the kind and operating conditions of individual transistors in the MOS microsystem was the subject of the tests presented in work (15). Attention is drawn there to the very essential fact that the change in the value of threshold voltage $U_{th}$ can be the measure of the progressive degradation of the MOS element leading to its failure. The sensitivity of this parameter to the changes in the physical state of the MOS element is confirmed also in work (16).

Reliability tests on linear self-contained microsystems require a more individualized (diversified) approach to the methods in which they are conducted, depending on the function which the given microsystem performs.

Self-contained microsystems with large scale integration, e.g., RAM memory circuits, cause additional difficulties in the course of testing. With respect to their complexity a thorough testing of all combinations of the input formulae is not usually possible, and likewise a guarantee of definite initial reliability of the microsystem or also a verification of the complete correctness of its operation after a certain period of operation (or testing) (17).

A definite alternative is to place on siliceous plates along with the microsystems, special test structures produced in the same technological process and later becoming the subject of reliability tests.

It can be stated with great approximation that the majority of the standard reliability tests carried on now on digital self-contained microsystems are being conducted using the following methods:

-- testing at an increased temperature (most often 125°C) with barrage polarization of the microsystem (HTRB),

-- dynamic testing (impulse operation) at 125°C or less,

-- storage (without polarization) most often at 125 or 150°C.

The first of the given methods seems to be the most effective and economical with consideration to the cost of the testing apparatus.

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## KEY TO FIGURES

Figure 1. Results of accelerated tests on sample tested in Group A and comparative sample.

Figure 2. Results of accelerated tests on sample tested in Group B and comparative sample.

Figure 3. Results of accelerated tests for stress with direct current and constant voltage.

Figure 4. Failure rate for bipolar and MOS microsystems. The data from laboratory tests is extrapolated to 55°C (the top boundary of the confidence interval is on a 60% level).

Figure 5. Dependence of failure rate for MECL 10,000 microsystems on the temperature in various operating conditions. The straight line signifies results for normal products, the broken line--for products undergoing burn-in.

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